Analogue Design
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Bipolar Amplifier Design
Part 3
Amplifier Biasing

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Abstract

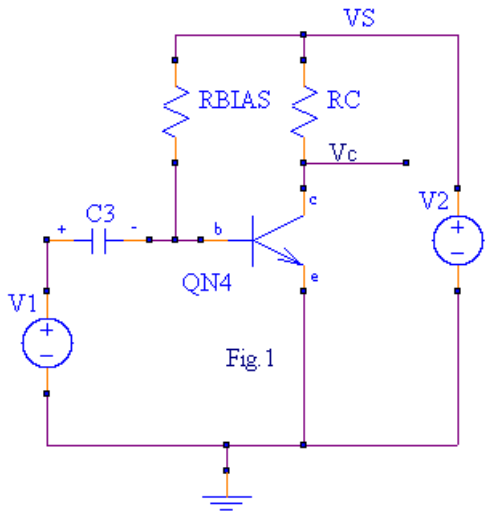
This paper leads on from paper 1, basic bipolar analog design and addresses DC biasing of basic transistor amplifiers.

The biasing problem is to set up correct steady state voltages and currents, irrespective of variation's in transistor characteristics and operating temperature.

Biasing

It is noted that the hfe, and the collector current for a given Vbe, of a transistor varies significantly from device to device, and over temperature. The bias circuit must reduce these variance to reasonable levels.

The first circuit to discuss is the simplest, and one that does not work in practice. Never use it!



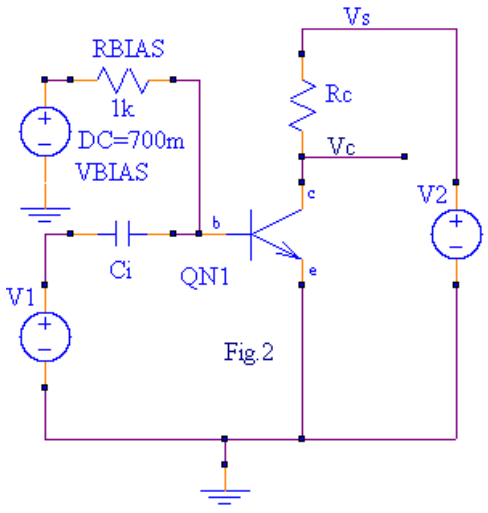
The idea here, is that RBIAS feeds base current thereby producing a collector current. The ac input signal is superimposed on top of the dc Vbe via the capacitor.

Suppose it is desired to have the static collector voltage at 1/2 the supply, and suppose that the supply was 10V. This would mean that Rc should drop 5V. Suppose further that the desired collector current is 1ma. This would result in an Rc of 5/ma = 5K ohms.

Now further assume that the hfe is 100. The base current would then be 10ua. Therefore to set the base current, rbias would have to be (10-0.7)/10u = 930k. However, if the transistor was another device of the same type, it might have a hfe of say 200. Since the base current remains constant in this circuit, it would

try and force a collector current of 2ma, casing a drop of 10 volts across Rc. There would be thus zero volts across the transistor. This would be one messed up operating condition!

Another unusable circuit. Never use this one as well!



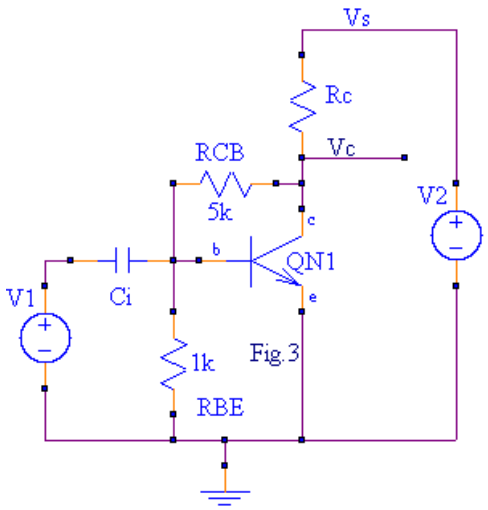
Suppose that RBIAS is low enough such that its ib.RBIAS voltage drop is small. VBIAS is then essentially the base emitter voltage Vbe. From paper 1, this current is given by:

$$I_e = I_o e^{\frac{V_{be}}{V_t}} \qquad -1$$

The issue here, is that I_o varies from device to device, typically by factor of ten or more. Therefor, if VBIAS was chosen to set the emitter current at say 1ma, another device in the same circuit might have 10ma of emitter current. Temperature variations would give further errors.

Now, a circuit that does work. This circuit is called the

Vbe Multiplier



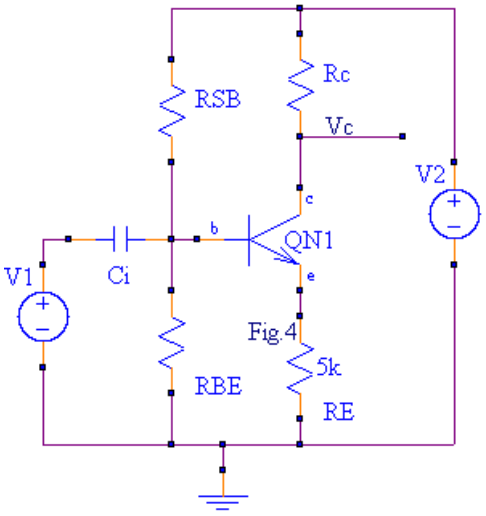
It was noted in prior papers that Vbe only change 60mV for a 10:1 change in emitter current. i.e. Vbe is approximately constant. If the base current in Fig.3 is a small fraction of the current through RBE, then it can be seen that RCB and RBE form a potential divider from the output collector. This means that:

$$V_o = V_{be}\left(1+\frac{R_{bc}}{R_{be}}\right) \text{-2}$$

This circuit is a *negative feedback* circuit. If Vo is initially too high, it will produce a larger Vbe via Rbc and Rbe. This larger Vbe will tray and force a larger current through Rc which will in turn tend to reduce Vo. This approach forces the collector voltage, and since the supply is fixed, the emitter/collector current is therefore fixed by (Vs-Vc)/Rc.

Equation (2) shows that Vo will only change in proportion to the delta(Vbe)/Vbe. That is, if Vbe is unknown within say 20mV, the error in setting Vo will be 20mv/0.7 ~ 2.8%. This is certainly an improvement on the last two circuits by an order of magnitude. The disadvantage of this circuit is that Rbc and Rbe may make the input resistance rather low for some applications.

Fixed Base Bias

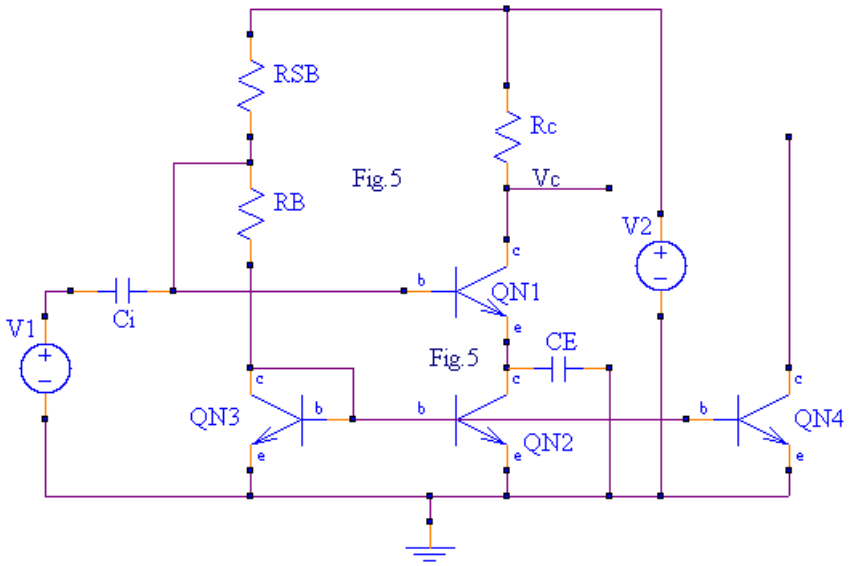


Assuming that the base current is small compared to the current through RBE, the voltage at the base node will be:

$$V_b = V_2\frac{R_{be}}{R_{be}+R_{sb}} \quad \text{-3}$$

Lets say the voltage at the base is set to 1.7V. This means that the emitter voltage will be 1v +/- any difference that Vbe has from 0.7. Once again, a 20mv/1V error is only 2%. Since the voltage at the emitter is now fixed, the emitter current will now be Ve/Re, hence the collector current and voltage will be deterministically set.

Current Source or Current Mirror Bias



In this circuit the voltage at the base (QN1) can vary significantly without effecting the emitter/collector bias current. RSB and RB are chosen that a suitable voltage is at the base, say 1V to 2V, so long as it is less then the voltage desired at the collector, less some, to avoid bottoming (clipping).

There is a current forced into the diode connected transistor QN3 of (V2- Vbe)/(RB+RSB). This current will be essentially independent of the Vbe of QN3, i.e. say within 20mv/10V ~0.2%. By assumption, QN2 is *matched* to QN3, so it will therefore try and force the same current through QN1, irrespective of QN1's base voltage. The voltage at QN1's emitter will automatically be forced to give the correct Vbe for QN1.

This current mirror technique is universally used in I.C. designs. Typically there is one master bias source that is mirrored to many transistors to bias all of the transistors in the design.

Website last modified 30th August 2013

www.kevinaylward.co.uk
