Analog Design
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Operational Amplifier Design
Miller And Cascode Compensation

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Overview

This paper presents an operational amplifier design example which forms a rebuttal to a typical understanding held in the literature and commonly expounded in text books, and commonly taught in university courses on amplifier design. This is the notion that capacitor feedback compensation to the low impedance point of a cascode driver stage is inherently able to produce *much* faster amplifiers than that of the standard Miller compensation technique. Some authors claim up to a 10 times improvement in bandwidth. This paper shows that such a free lunch by the simple process of moving one feedback connection is not supported for the facts.

Introduction

The literature on amplifier feedback typically presents what can only be regarded as an enormous mess of equations, ostensibly proving that compensation to the low impedance point of a cascode driver amplifier eliminates a right half plane zero and hence can result in a vastly improved compensated bandwidth of the amplifier. Actual real design of *optimised* real amplifiers shows that, although significant improvement in PSR is often achieved, any improvement in BW is relatively marginal.

A fundamental issue in comparing amplifier topologies is that of comparing apples to apples. It is absolutely crucial that the amplifiers are *designed correctly*. This means paying extensive attention to the operating conditions of all transistors and choosing the *correct* sizes for all transistors, in particular paying particular attention to W/L, WL, gds, V_{gts}, V_{dsat} V_{ds}, *over all process corners and temperatures*. It is easy to have a bad design, and then claim that it is improved by doing something different. Furthermore, blanket conceptualisations take no account of other design features that may be added, for example, additional RC networks, and additional active devices.

To be quite frank, it might be stated that novice PhD students, *typically* do not have the knowledge and experience to perform optimal analog design. Indeed, Rich Beyer (ref 4, CEO Intersil) states with regard to the ability of newly minted analog design engineers "…It takes five to six years for them to be able to do a design on their own…".

Real commercial, viable analog design, by professional engineers, is performed by running *extensive Spice simulations and optimisations by Spice simulations*. Despite the extensive production in university courses, of equations several pages deep, these equations are in fact, completely useless for real commercial design. They are simply way too complicated. They use far too many approximations to the real circuit to give an accurate understanding of how the circuit is really operating, and nobody actually uses them in the real commercial world, which is the world that matters!

This may be compared to gaining an understanding of colliding, rotating charged black holes within General Relativity. It's rather hard without computers.

Reference Example

The example chosen here is simply an example to hand, presented by Boise State University (ref 5) to illustrate that what may be claimed as an improvement by the technique of cascode compensation, when compared to an optimised Miller design in an equivalent process at guestimated similar operating voltages and currents, and accuracy.

The reference example is the set of Miller and cascode compensated amplifiers given by ref 5.

Issues with the comparison are:

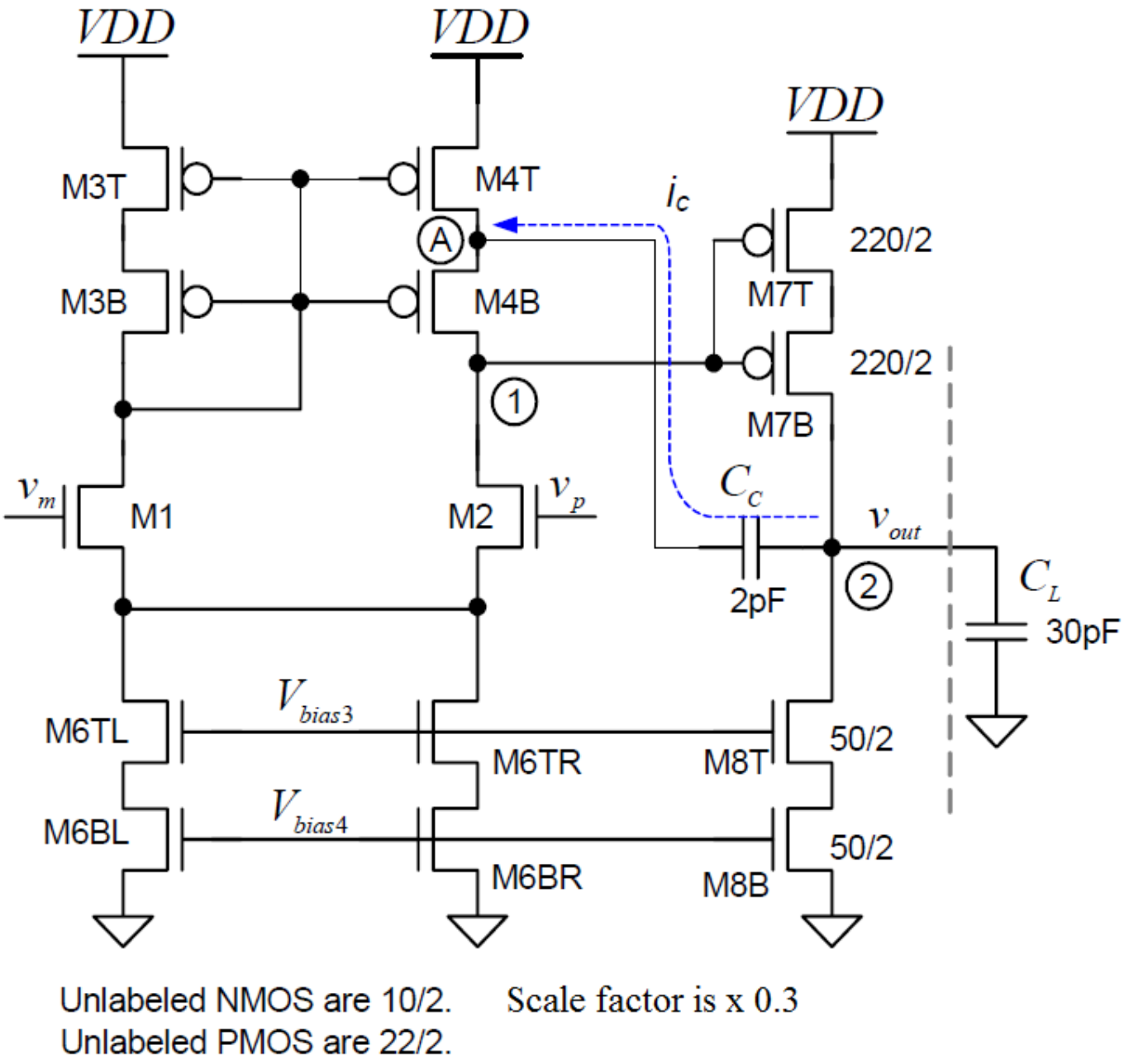
1 – Input common mode voltage range is not specified

2 – Standard deviation of input offset voltage is not specified.

3 – Results over process corners and temperatures are not specified.

Comments - The reference example is described as being designed specifically for low voltage applications so common mode range is very important. The actual design has a diode in the source of the input transistor and so its input common mode is extremely unlikely to include the power supply. LV designs, by definition, are usually taken to have a common mode range that includes at least one of the supply rails. Offset voltage is also crucial as it dictates the size of the transistors. Smaller transistors are faster but have larger offsets.

Reference Cascode Compensated Schematic



Note all sizes are scaled by 0.3, e.g. the input pair is actually 6.6u/0.6u

Specifications for this example schematic are:

Op-amp Topology	A_{DC} (dB)	f_{un} (MHz)	C_C (pF)	PM	t_s (ns)	Power (mW)	Layout area (mm^2)
Miller	57	2.5	10	74°	270	1.2	0.031
Miller with R_Z	57	2.7	10	85°	250	1.2	0.034
SLCL (this work)	66	20	2	75°	60	0.7	0.015
SLDP (this work)	60	35	2	62°	75	0.7	0.015

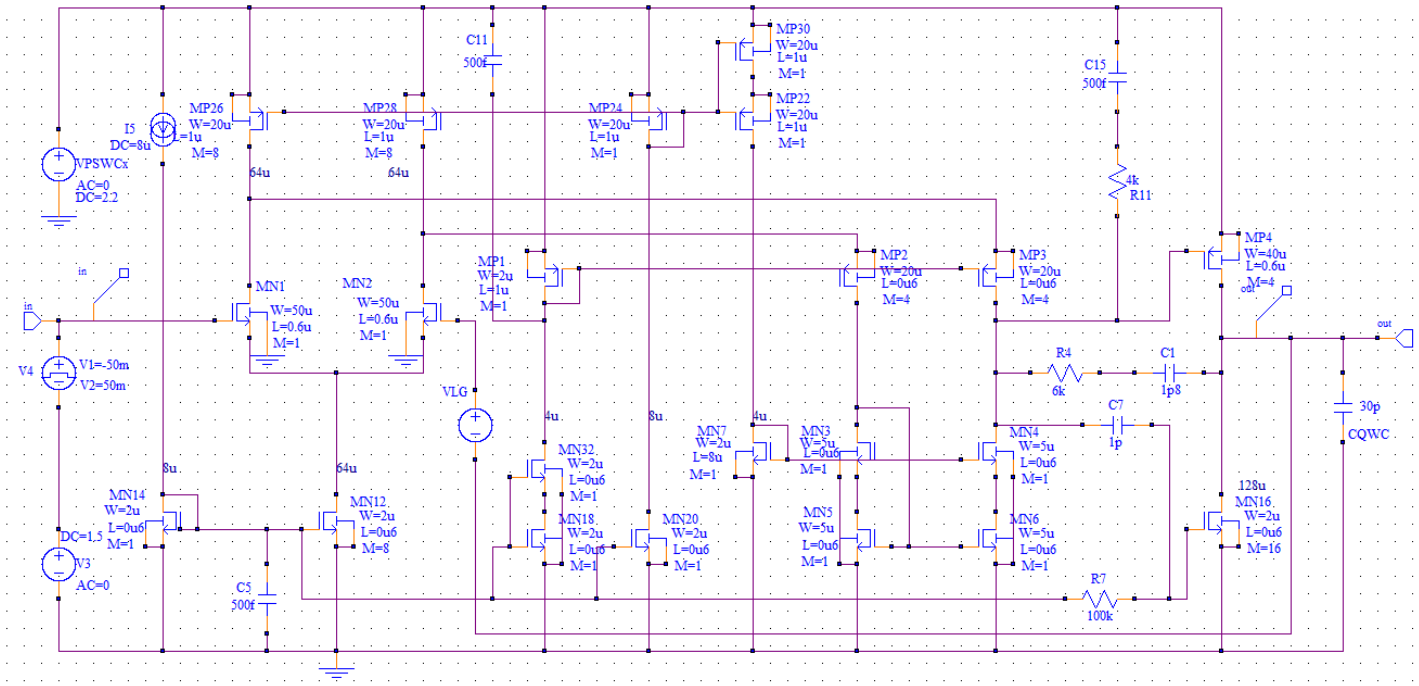
The SLCL and SLDP being the low impedance feedback point compensation topologies (see ref 5/6). Load capacitance is 30pf. Extrapolation from the reference documents (ref 6) indicates possibly Idd~280ua.

Worst case results for the reference design are anticipated to be significantly different from the above table. Indeed, it is not known whether the reference design is stable over all process corners. Typically, simulations have shown that cascode compensated amplifiers may have significant stability issues.

Miller Compensated OpAmp

A nominal Miller amplifier was developed in an XFAB BiCMOS 0u6 process, as shown:

Fig. 1



Note the special use of the capacitor coupling the driver stage to the constant current output class A load. This allows the output stage to sink an order of magnitude larger current for transients. It also increases the loop gain and stability margin a tad. The small RC damping network is for stability when the load is only a few pf. It can be eliminated if it is known that the load has a minimum value, say 10 pf. The input stage also has a larger gm than the reference design, and with an increase in area in order to keep the input offset voltage lower. Additionally, it is a true low voltage design, being a standard folded cascode with much superior input and output signal handling capability. The reference design has its output device limited by its input pair clamping

its gate drive. In reality, the reference has severe limitations as a “low voltage design”. It saves the current of the fold, but essentially, this makes it of no real use in a commercial product. Even if it were true that cascode compensation could give a significant advantage, the optimal option would be to use this Miller amp configured as a cascode compensated amplifier.

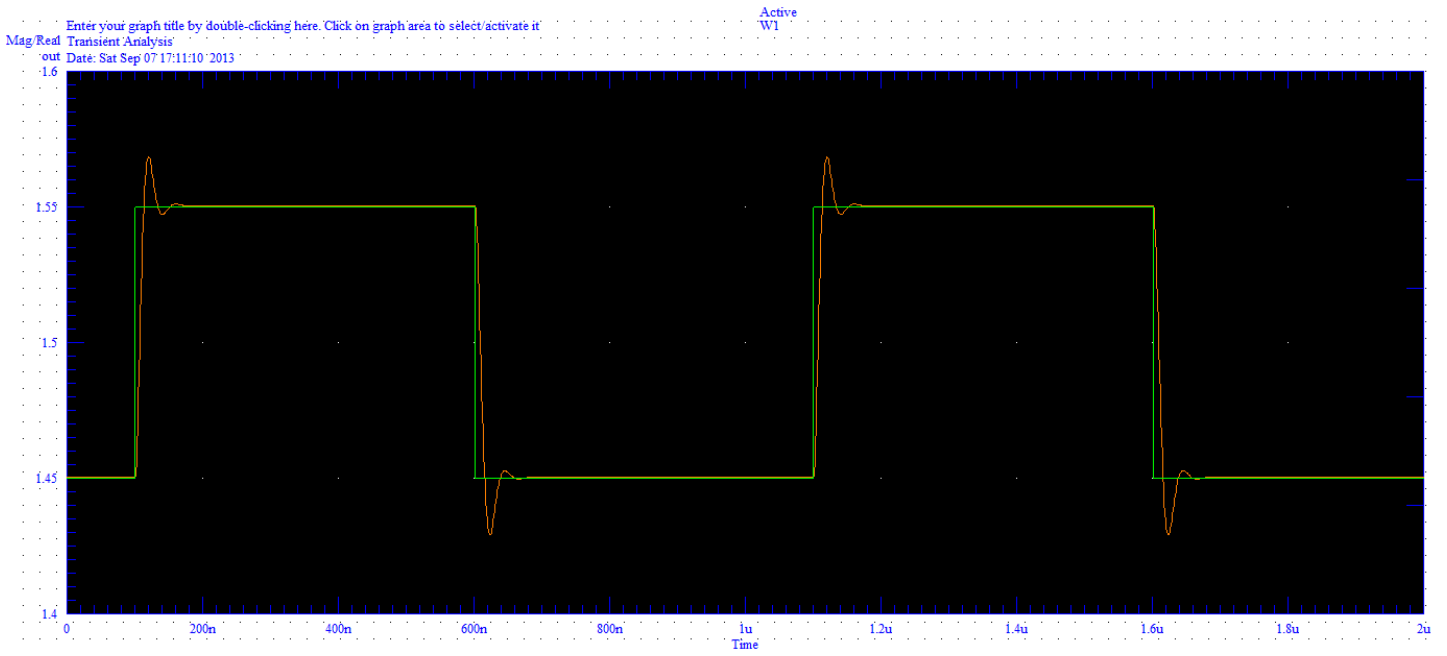
Miller Results Tables

Topology	A_{dc} (dB)	F_{un} (MHz)	Cc (pf)	PM	t_s (ns)	Power (2.2V) (mW)	I_{vdd} ma	VCM	Area (mm^2)
Miller Rz	85	22	1.8	49	70	0.64	0.29	1.5-VDD	<0.015

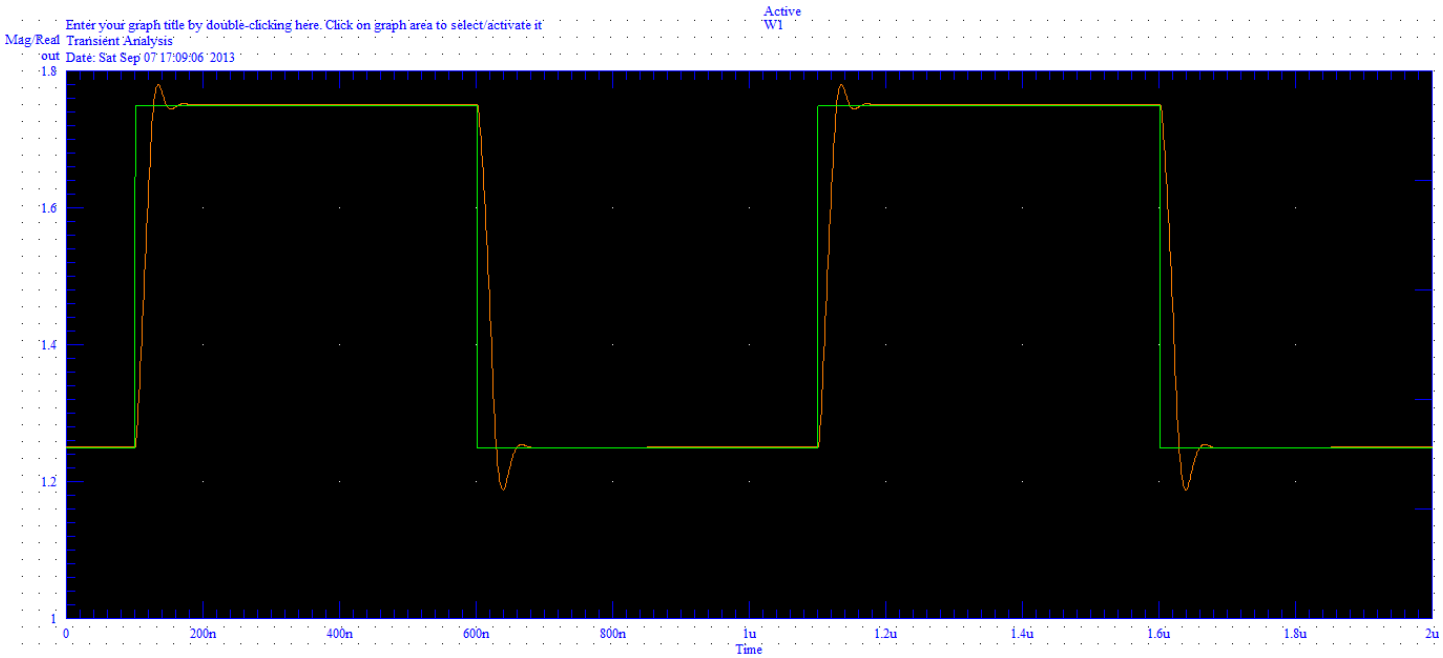
Note: LF loop gain is nominally 85 dB, which is an order of magnitude greater than the reference design.

These nominal results confirm that the performance is on a par to that of the example cascode compensated reference design.

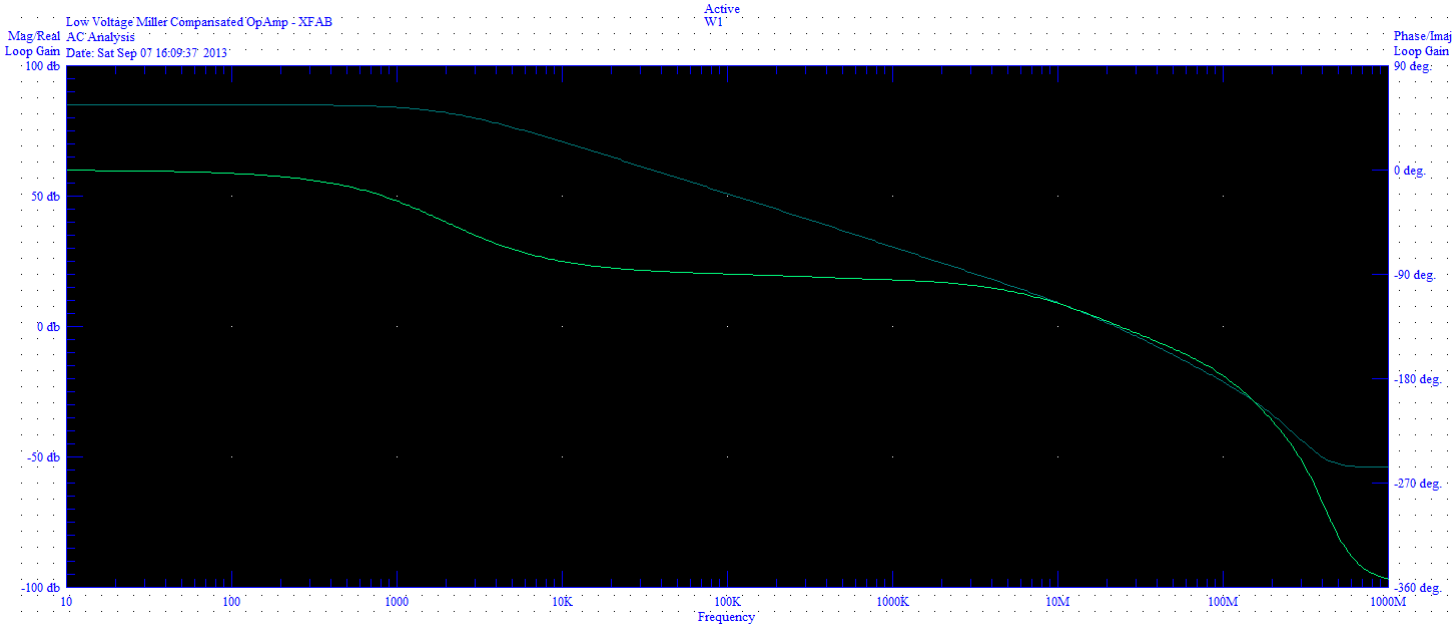
Nominal Transient – 100 mV Input



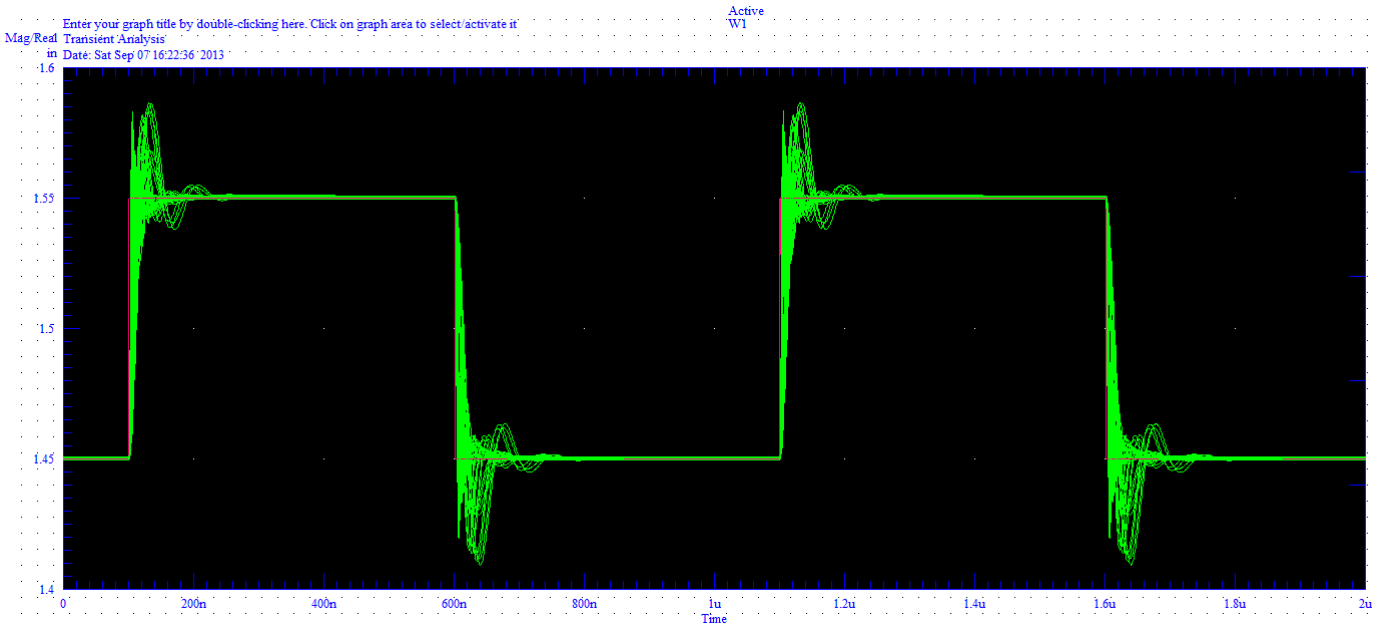
Nominal Transient – 500 mV Input



Nominal Loop Gain



Worst Case Corners Transient – 100 mV Input



Worse case results are provided to show, principally, that this Miller compensated example, is stable over various capacitive load conditions. These simulations run from a load capacitance from 2p to 40p, temperature from -40 degs to 125 degs, and all combinations of process corners.

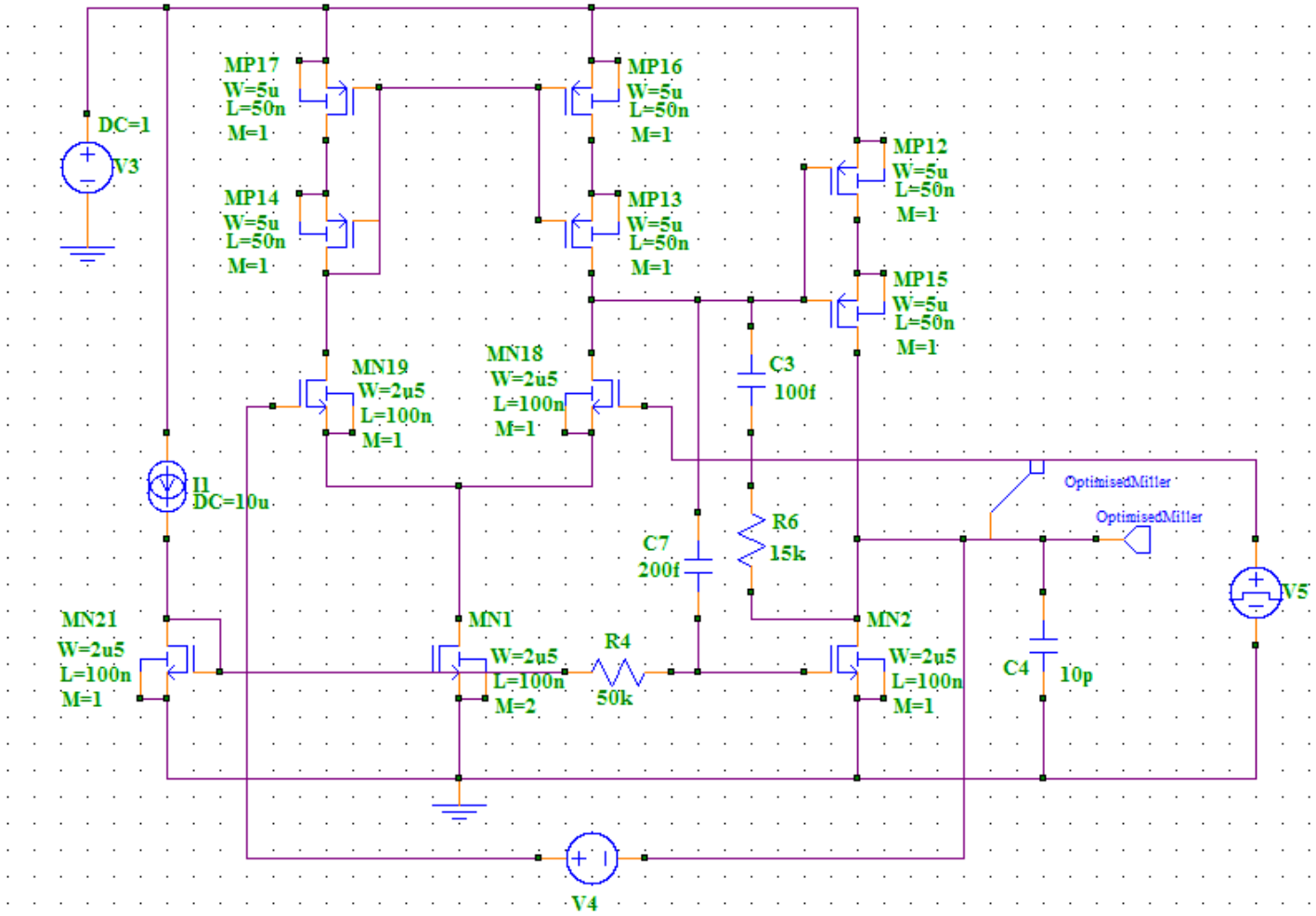
Conclusions

A worst case simulated Miller compensated design has been presented that, by and large has the equivalent performance to the cascode compensation reference design, in contradiction to the many claims from the many noted academic references. Extensive practical experience in the simulation and design of operational amplifiers clearly leads to the result that there is no such thing as a free lunch. Whilst, in some circumstances there may be some improvement in a cascode compensated bandwidth, the high ratios of 10:1 improvement, sometimes claimed, can not be supported by the facts. If this were so, presumably some clever dude could take this Miller design and convert it to say, one of 100 MHz unity gain bandwidth, at similar performance and power, rather than its 20 MHz. If so, please contact the author, and a crate of Guinness will wing its way to them.

Addendum – March 14th 2015

Partly in response to this paper, a follow-up was made at Bad Circuit Design 12 (BC12) further proposing the view that Miller compensation was “bad design”, and that additional topology changes would still result in an “indirect” design that was “4 to 10 times faster” than a Miller design, and be 10 times larger in capacitor size such as “240 ff compared to 2.4p”. However, the example chosen to illustrate that proposal has a structure that could be significantly optimised.:

Optimised Bad Circuit Design 12 Schematic



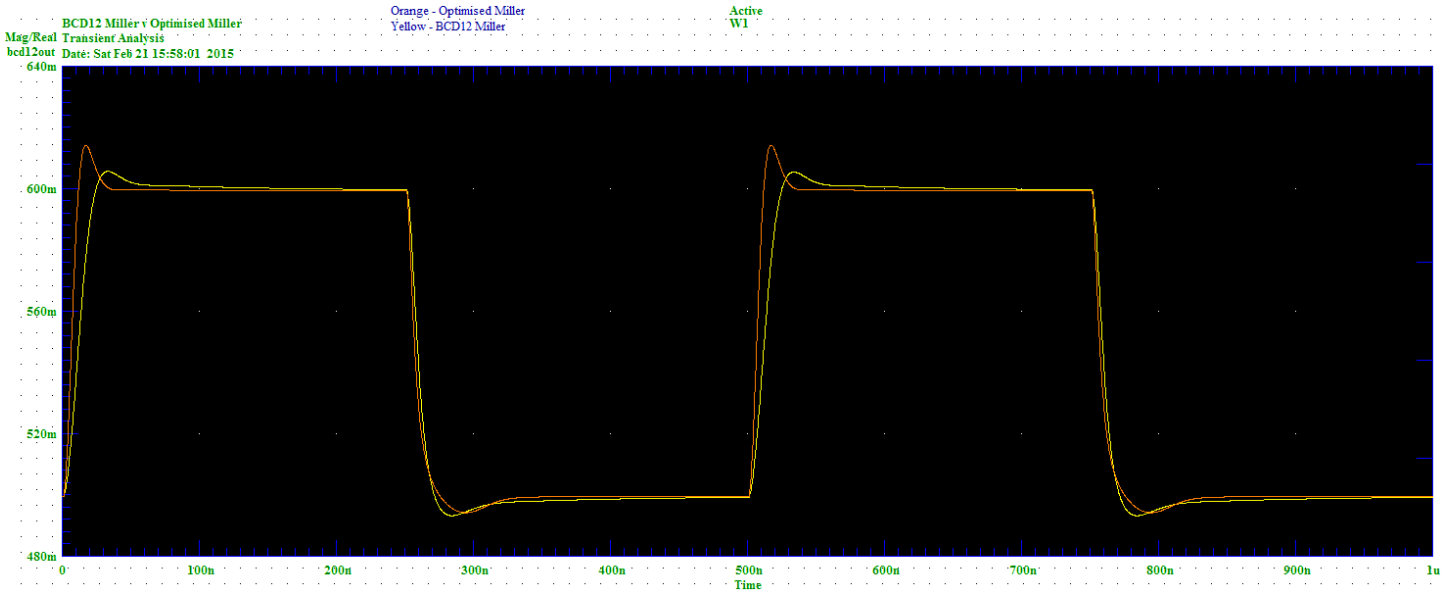
Notes:

Significantly smaller compensation capacitor.

Significantly smaller AB boost capacitor.

Removal of the BC12 extraneous RC network.

BCD12 Reference Graph And Optimised Miller Graph

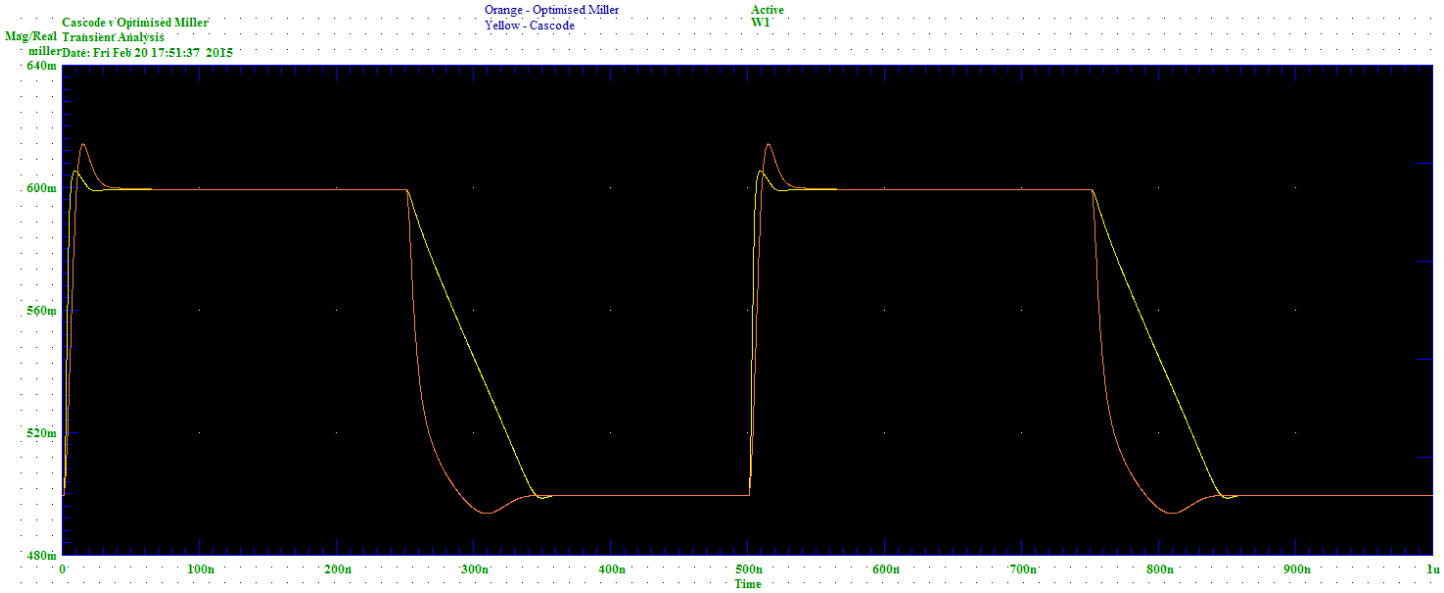


Yellow- Original BCD12 Miller with AB boost

Orange – Optimised Miller with AB boost

Notes: Optimised Miller is notably faster on leading edge

BCD12 Cascode and Optimised Miller with AB Boost Waveforms – CL=10pf



Yellow- Original indirect, cascode compensated topology

Brown – Optimised Miller with AB boost topology

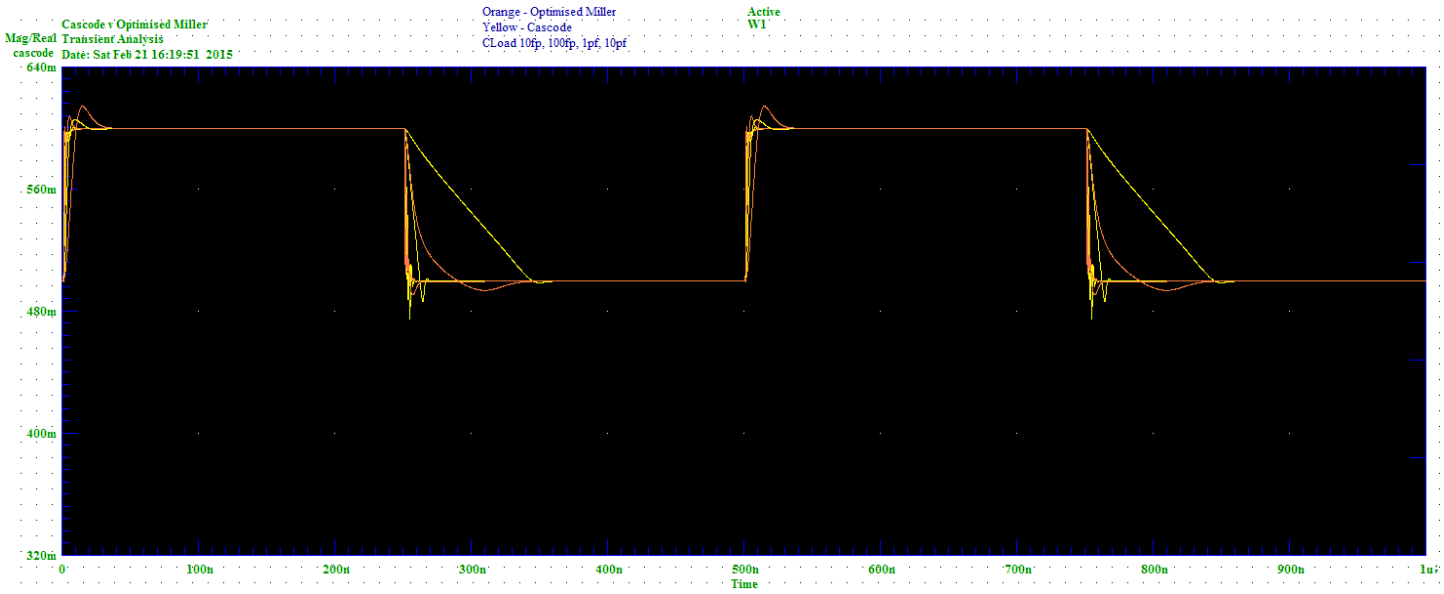
Notes:

Optimised topology has a much closer rising edge match to the BCD12 cascode than the original BC12 proposed Miller topology.

Optimised topology is drastically faster on trailing edge than the BC12 cascode topology, without AB speedup.

AB Speedup for the cascode topology does give similar trailing edge improvement, but is not shown here.

Optimised Waveforms Stability – CL=10f, 100f, 1pf, 10pf



Notes:

Stable at all loads.

Summary: In many cases a cascode compensation method is the preferred choice, typically allowing for a faster response and superior power supply rejection. However, if topologies have been optimised, in this authors opinion, any speed up greater than a factor of 2, is dubious, and would indicate that the design has not been optimised. Additionally, there are circumstances where the Miller option, is a more optimum choice. The afore mentioned crate of Guinness offer is still open…

Oh…the BCD12 design, is running in severe subthreshold, has dynamic range and non-linearity issues, and thus would fail most commercial design reviews let alone a final tape-out review, but that is another story…

References

1 – "Analysis and Design of Analog Integrated Circuits" –Grey, Hurst, Lewis and Meyer
2 – "Design of Analog Integrated Circuits" – Behzal Razavi
3 – "CMOS Circuit Design, Layout, and Simulation" – Jackob R. Baker
4 - http://www.electronicsweekly.com/news/components/analogue-and-discretes/good-analogue-design-is-key-to-success-says-intersil-2006-06/
5 - "High-Speed Op-Amp Design: Compensation and Topologies for Two and Three Stage Designs," http://cmosedu.com/jbaker/papers/talks/Multistage_Opamp_Presentation.pdf -Saxena, V., and Baker, R. Jacob, (2007-2008), presented at various universities and companies.
6 - Indirect Feedback Compensation Techniques for Multi-Stage Operational Amplifiers - Vishal Saxena
7 - http://cmosedu.com/cmos1/bad_design/bad_design12/bad_design_12.htm

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Website last modified 14th March 2015
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