Analog Design
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Obtaining Oscillator Loop Gain & Phase
Of
Common Emitter Oscillators

Back to Contents

Overview

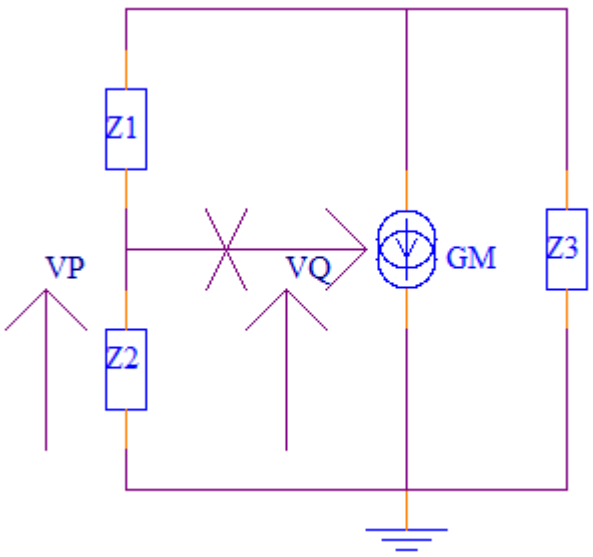
A single transistor oscillator may be configured as a common emitter (Pierce), common collector (Colpitts) or topology. These topologies are identical in the sense that identical circuits, with only the ground connection moved, have exactly the same loop gain and identical currents in all device terminals, with only the voltages with respect to ground being different. However, a cursory analysis of the configurations shows a somewhat paradoxical situation where it initially might appear as if the loop gains for the topologies are different.

This paper illustrates the issues involved and provides a correct analysis of the loop gain, and how to actually perform a loop phase/gain analysis of the common emitter topology using SPICE

Analysis

A general transistor oscillator block diagram is shown in Fig. 1:

Fig. 1 – General Single Transistor Feedback Oscillator Topology



In Fig. 1 the X represents a break in the feedback loop from where to calculate the Return Ratio (RR) or Loop Gain. VP/VQ represents this RR. The following forms an analysis of the loop:

To simplify the expressions, the load across the voltage controlled current source, GM, is first defined as ZL.

$$ZL = \frac{(Z1+Z2)Z3}{Z1+Z2+Z3} \quad (1.1)$$

Next, the potential divider action of Z1 and Z2 to obtain VP is expressed as:

$$\alpha = \frac{Z2}{Z1+Z2} \quad (1.2)$$

With the voltage across Z1 given by the ratio (1-α)

The voltage across ZL is given by the negative of the total current from the GM source into ZL, that is:

$$V_{ZL} = -GM.VQ.ZL \quad (1.3)$$

Hence VP is expressed as:

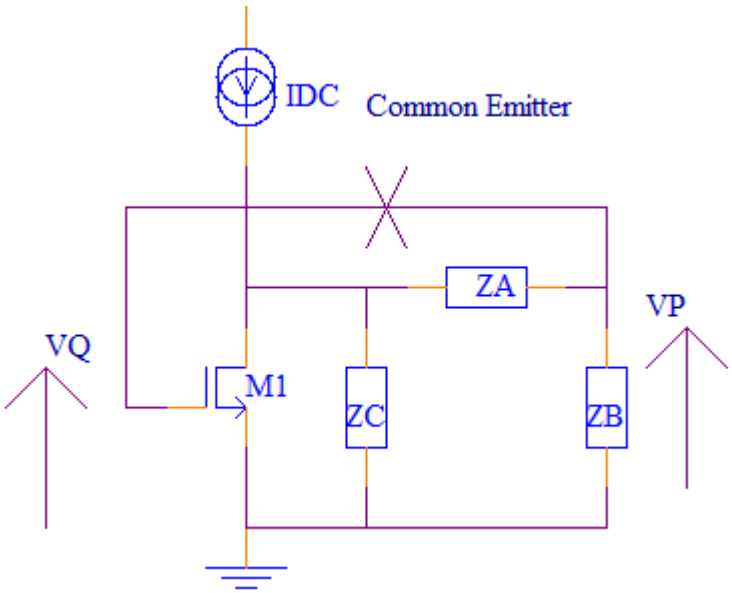
$$VP = -\alpha GM.VQ.ZL \quad (1.4)$$

Whence the RR is given by:

$$RR = -\alpha GM.ZL \quad (1.5)$$

Consider the common emitter topology:

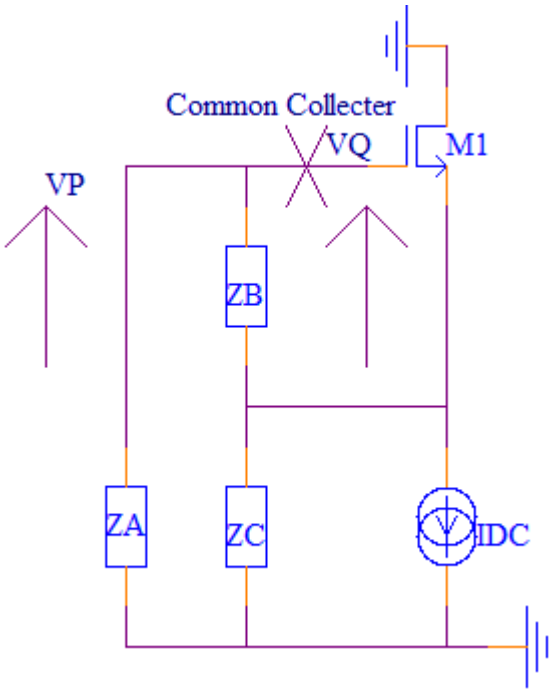
Fig. 2 Common Emitter Topology



From inspection, it is seen that general oscillator topology immediately applies to this common emitter oscillator such that equation 1.5 represents the correct return ratio for this topology.

Now consider the emitter follower/common collector topology:

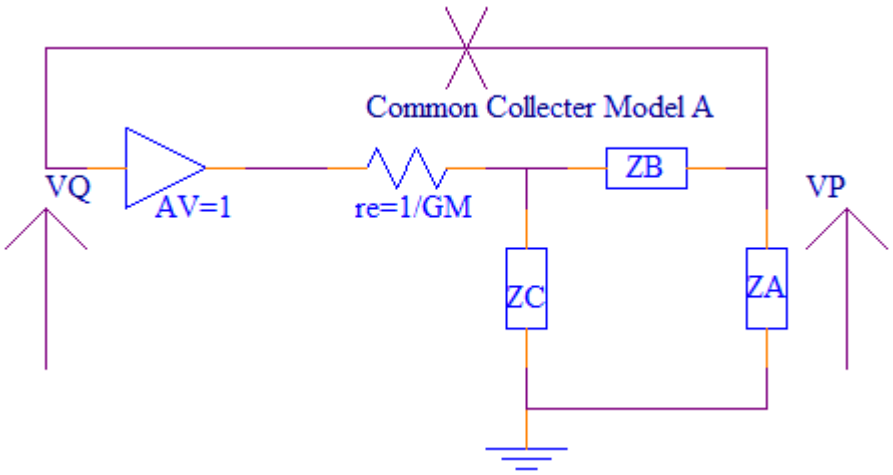
Fig. 3 Emitter Follower Topology



Note that ZB (Z2) is the impedance *across* the gate/source for *both* topologies.

To analyse the emitter follower topology, an initial approach might be to consider the following model:

Fig. 4 Emitter Follower Model A



This would be a typical approach to analysing most non feedback topologies. The emitter follower being simple replaced as a unity gain buffer with an output resistance equal to 1/GM. However, from inspection, this would result in a return ratio given by:

$$RR = (1-\alpha)\frac{ZL}{ZL+re} = \frac{(1-\alpha)GM.ZL}{GM.ZL+1} \quad (1.6)$$

Whence it is seen that 1.6 is not the same as 1.5. Indeed, a "by inspection approach" might conclude that as re is usually low, ZC might have a very small effect on the return ratio. This is not correct. Something has went wrong in the analysis, as it is certainly known from simulations, that common emitter and emitter follower oscillators, when appropriately configured, are identical. For example:

Fig. 5 – Common Emitter and Emitter Follower Oscillator Topologies

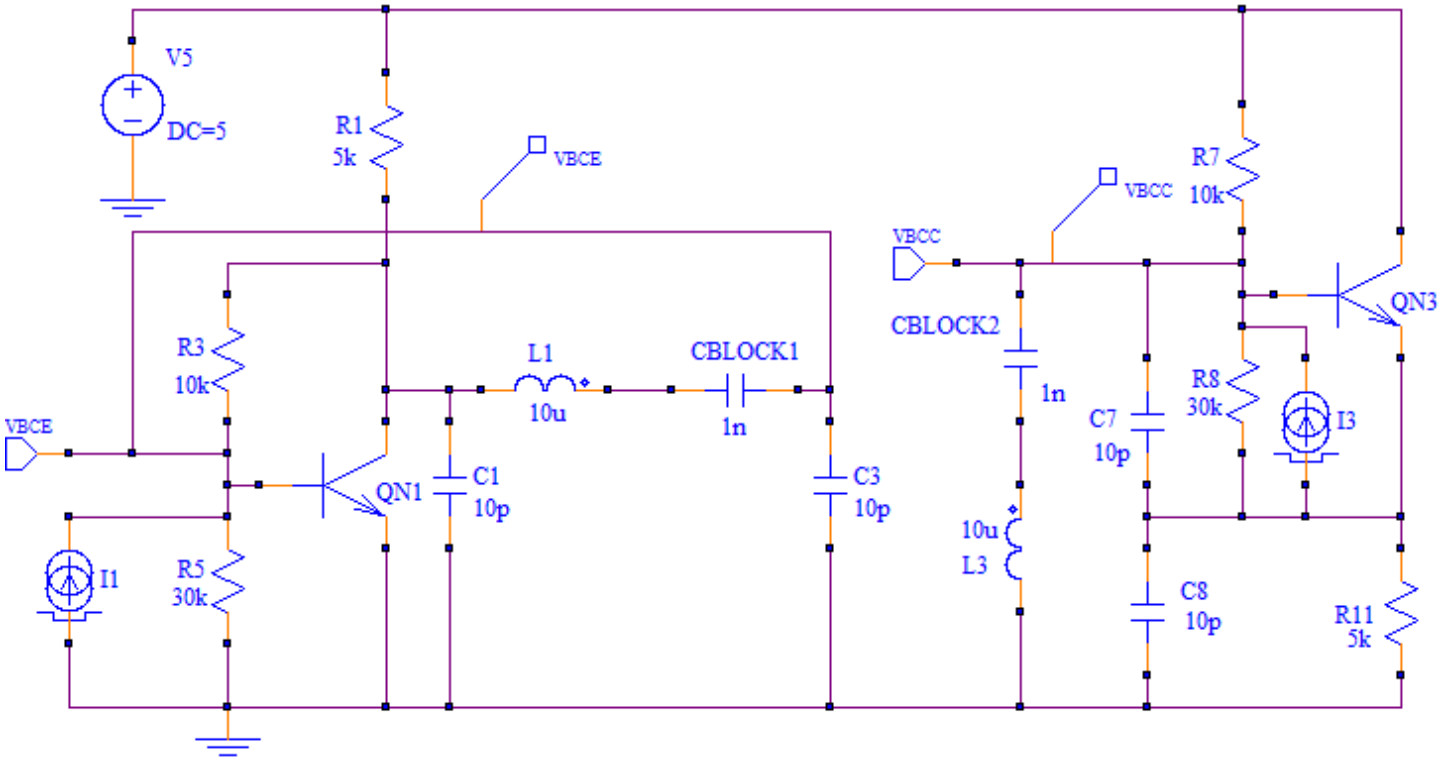
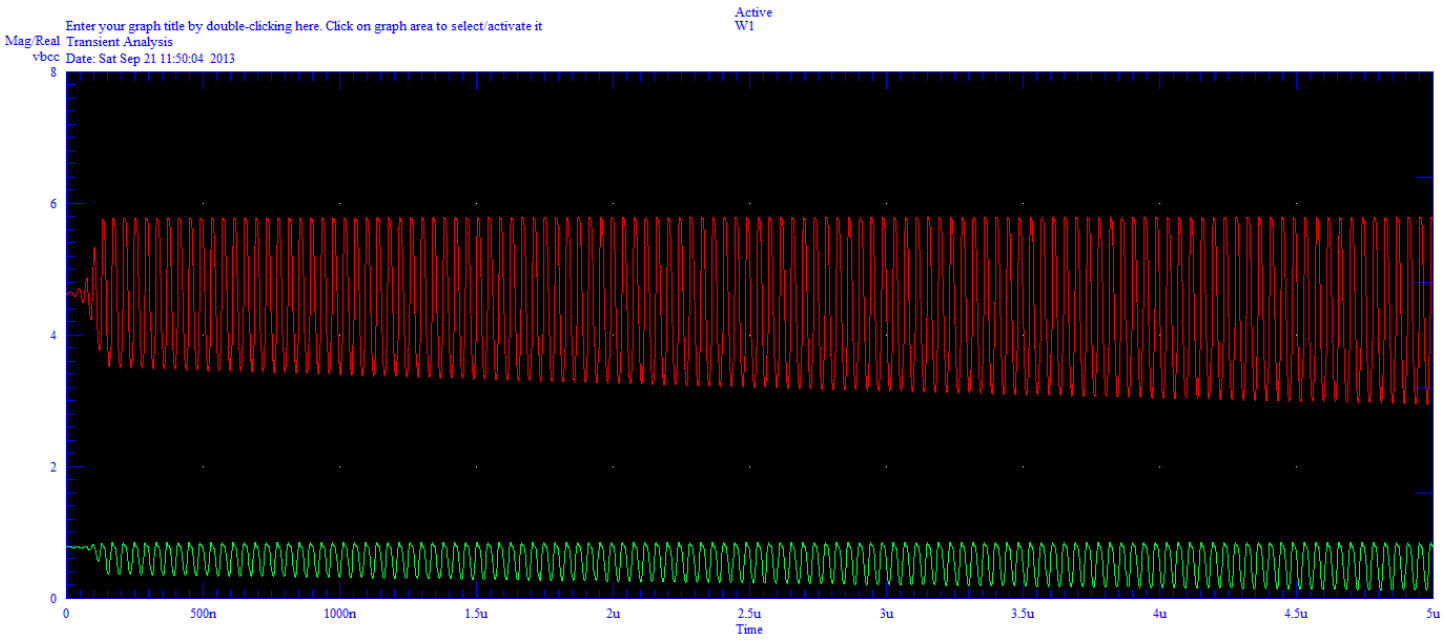


Fig. 5 is a schematic illustrating both common collector and emitter follower oscillators with identical operating conditions. The current sources are transient single pulse start up sources.

Fig. 6 Base Voltage Waveforms



It is noted that the voltage waveforms of the two topologies at the base with respect to ground are different.

Fig. 7 Collector Current Waveforms

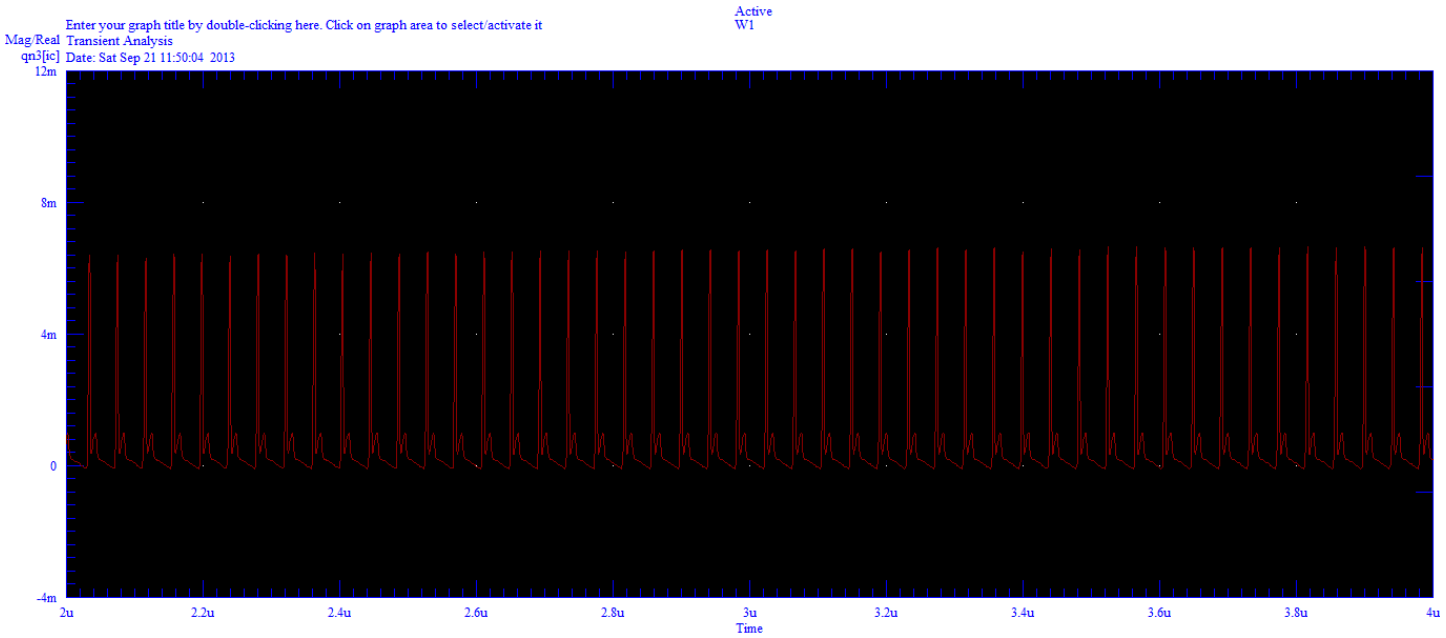
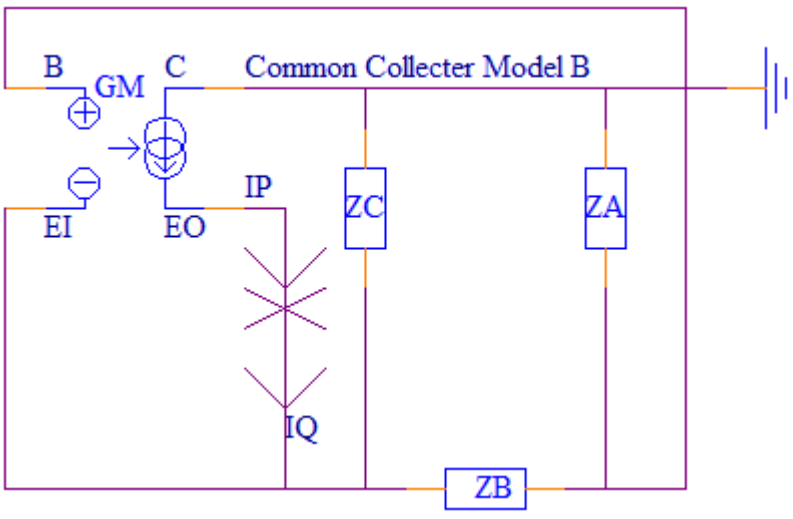


Fig. 7 plots two current waveforms from the common emitter and emitter follower topologies at once from SuperSpice simulations, however, the waves overlay perfectly, such that only one waveform is actually visible. This shows that the two topologies are identical with regard to fundamental operation.

Correct Analysis of the Emitter Follower Loop Gain

The root of the problem for the emitter follower model A, is that the model fails to account for the internal feedback of the emitter follower. It is a known property of stability analysis that a correct return ratio may only be calculated if *all* feed back loops are broken at once. To rectify this, the following model B may be constructed that breaks the implied internal connections at the emitter. The model achieves this by constructing an input emitter and an output emitter, and calculates the Return Ratio via currents rather than by voltages.

Fig. 8 Emitter Follower Model B



The voltage at node IQ, fed by the current IQ may be expressed as:

$$V_{IQ} = +IQ.ZL \quad (1.7)$$

The voltage across the input of the GM source, V_{be}, is the negative voltage across ZB, and may be expressed as:

$$V_{GM} = -\alpha IQ.ZL \quad (1.8)$$

Hence:

$$IP = -\alpha GM.IQ.ZL \text{ (1.9)}$$

So, the return ratio is given by:

$$RR = \frac{IP}{IQ} = -\alpha GM.ZL \text{ (1.10)}$$

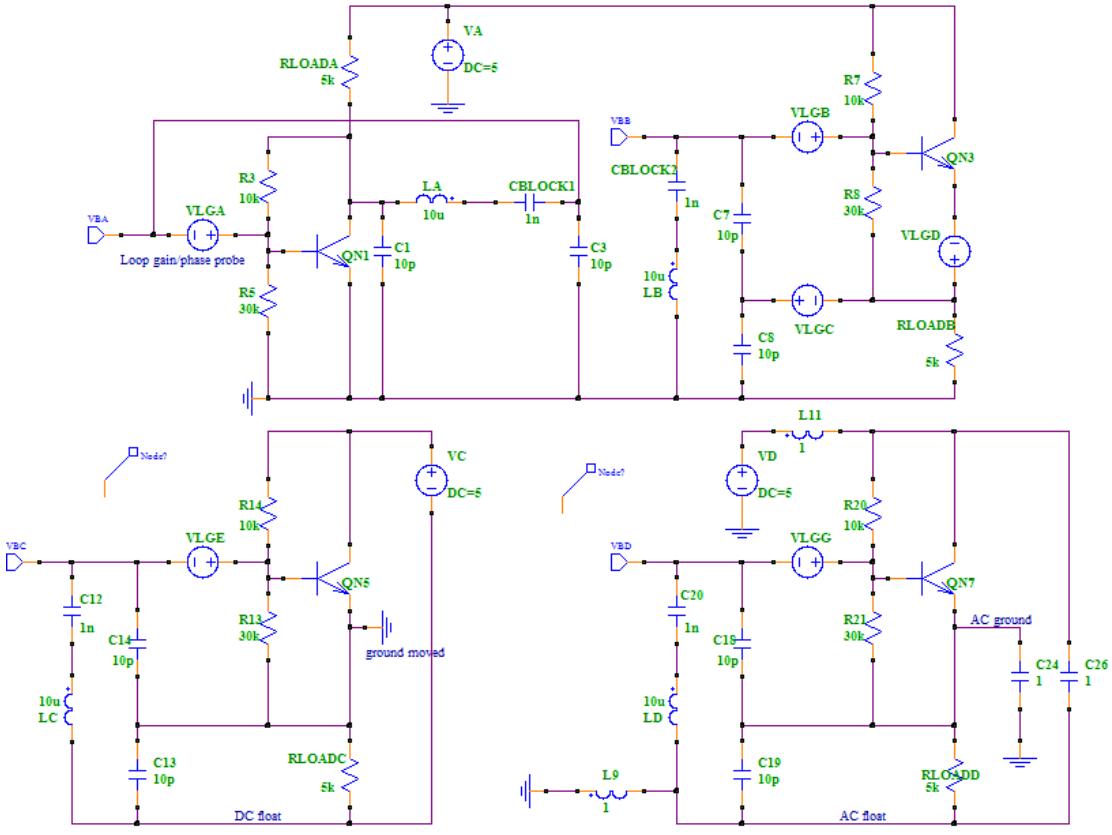
This is the same expression as for the common emitter topology.

Spice Loop Gain Simulation

The forgoing analysis shows that a direct attempt at calculating the loop gain for the common collector topology fails. Typical techniques such as that introduced by Middlebrook or Tian, of inserting a voltage source in the loop produces incorrect results.

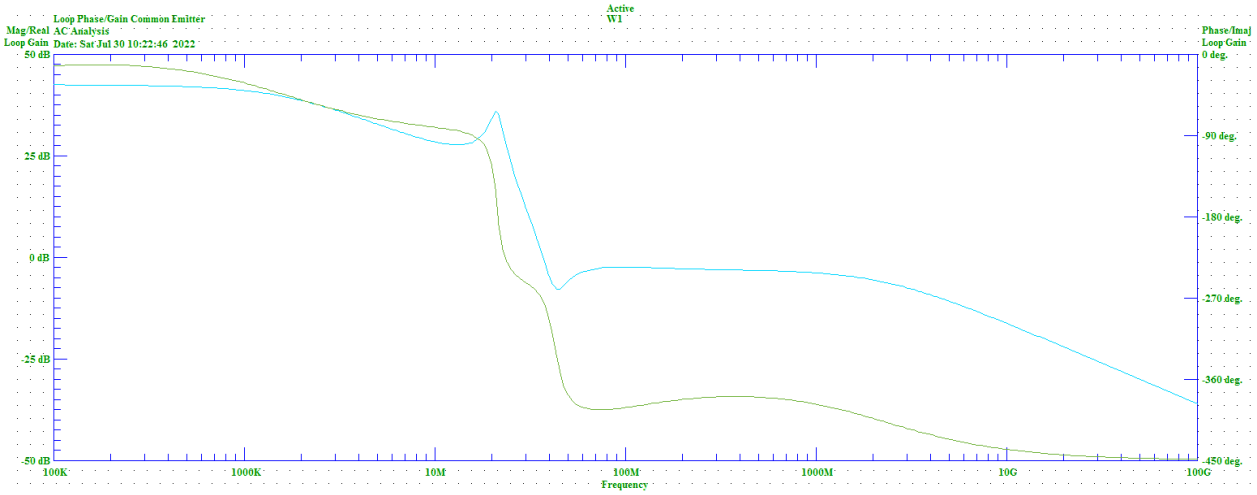
This problem may be solved, simply by either DC grounding or AC grounding the system so that the common collector topology looks “as if” it is a common emitter topology, as shown below.

Fig. 9



For the common emitter topology a loop analysis of the example schematics results in:

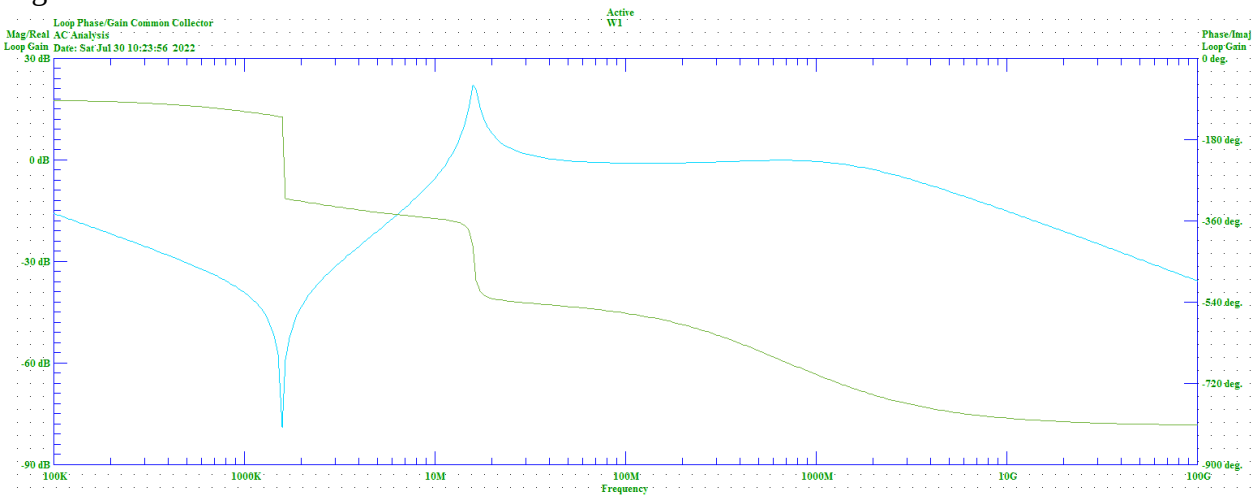
Loop Gain/Phase: Phase Margin=-89.2324Degs.
Loop Gain/Phase: Gain Margin=-34.9468dB
Loop Gain/Phase: Unity Gain Frequency=36.3078MHz
Loop Gain/Phase: Low Frequency Gain=42.53dB
Loop Gain/Phase: Zero Phase Frequency=21.8776MHz
Fig. 10



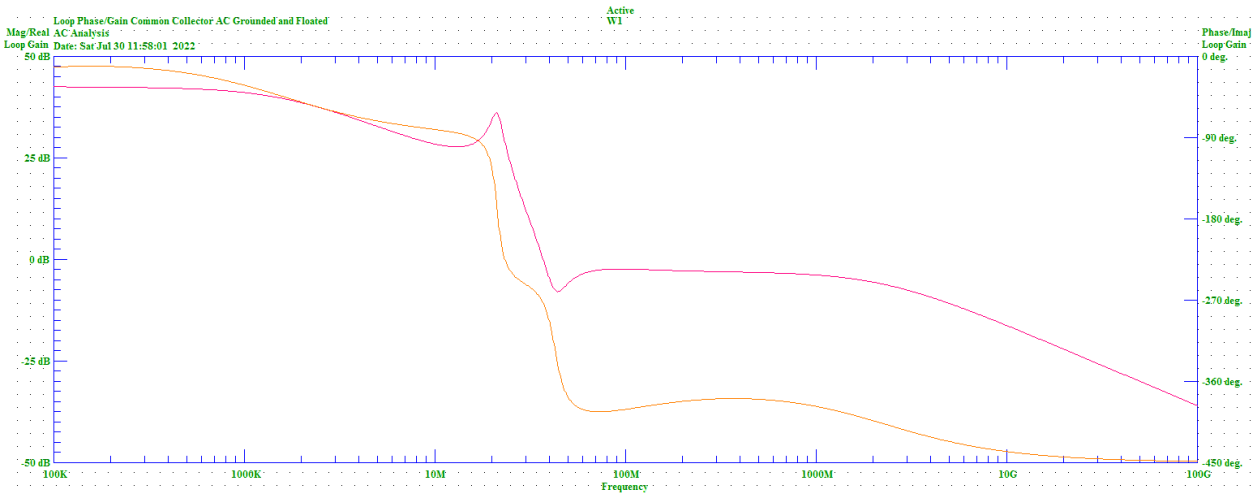
However, for the common collector topology a standard loop analysis results in different results, wherever the loop sense is placed, for example:

Loop Gain/Phase: Phase Margin=-367.726Degs.
Loop Gain/Phase: Gain Margin=58.8648dB
Loop Gain/Phase: Unity Gain Frequency=43.6516MHz
Loop Gain/Phase: Low Frequency Gain=-15.8131dB
Loop Gain/Phase: Zero Phase Frequency=1.65959MHz

Fig. 11



In contrast, loop gain analysis for either the DC or AC re grounded topologies produce identical results as the common emitter topology, as it should, as the topologies are electrically identical, except for the placement of the ground.



Summary

It has been shown that a cursory analysis of the loop gain/return ratio of the emitter follower oscillator may result in an incorrect determination of its RR. It has been shown that correct application of feedback stability theory resolves this initial paradox. It has been demonstrated that the loop gain and phase of the common collector topology may be obtained by repositioning the effective ground point.

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